What is Claimed is:

1. A setup/hole time control apparatus, comprising:

a driver for outputting a global bus line control signal by driving an output signal of an input buffer;

a signal delay unit for delaying the global bus line control signal selectively connected to the driver;

a decoding unit for outputting a test mode delay signal by decoding a test control signal for determining to control setup/hold time corresponding to the global bus line control signal, a test mode entry signal, and a test mode end signal; and

a delay control unit for controlling the setup/holde time of the global bus line control signal by selectively connecting the signal delay unit to the driver according to a state of the test mode delay signal.

2. The setup/hold time control device according to claim 1, further comprising a first latch for latching and outputting the global bus line control signal in synchronization with a clock signal.

3. The setup/hold time control device according to

claim 1, wherein the driver comprises an inverter chain for non-inverting and delaying an output signal of the input buffer connected in series.

4. The setup/hold time control device according to claim 1, wherein the signal delay unit comprises:

a first capacitor unit connected selectively to a first node of the driver by the delay control unit; and

a second capacitor unit connected selectively to a second node of the driver by the delay control unit.

5. The setup/hold time control device according to claim 4, wherein the first capacitor unit and the second capacitor unit are MOS capacitors.

6. The setup/hold time control device according to claim 4, wherein the delay control unit comprises:

a first delay control unit for delaying the setup/hold time of the global bus line control signal by selectively connecting the first capacitor unit to the first node according to a state of a first test mode delay signal; and

a second delay control unit for advancing the setup/hold time of the global bus line control signal by

selectively connecting the second capacitor unit to the second node according to a state of a second test moe delay signal.

7. The setup/hold time control device according to claim 6, wherein the first delay control unit comprises a first transmission gate and a second transmission gate for receiving the first test mode delay signal through a NMOS gate, and receiving the first test mode delay signal inverted through a PMOS gate to selectively connect the first MOS capacitor unit to the first node.

8. The setup/hold time control device according to claim 6, wherein the second delay control unit comprises a third transmission gate and a fourth transmission gate for receiving the second test mode delay signal through a PMOS gate, and receiving the second test mode delay signal inverted through a NMOS gate to selectively connect the second capacitor unit to the second node.

9. The setup/hold time control device according to claim 6, wherein the decoding unit connects the first capacitor to the first node by outputting the first test mode delay signal at a high level when the test control

signal is at a high level, and intercepts connection between the second capacitor unit and the second node by outputting the second test mode delay signal at a high level when the test control signal is at a low level.

10. The setup/hold time control device according to claim 9, wherein the decoding unit comprises:

a logic unit for logically operating the test control signal and the test mode entry signal to output a first output signal and a second output signal;

a second latch for latching the first test mode delay signal according to the first output signal and the test mode end signal; and

a third latch for latching the second test mode delay signal according to the second output signal and the test mode end signal.

11. The setup/hold time control device according to claim 10, wherein the logic unit comprises:

a first NAND gate for NANDing the test control signal and the test mode entry signal to output the first output signal; and

a second NAND gate for NANDing the test mode entry signal and the inverted test mode entry signal to output

the second output signal.

12. The setup/hold time control device according to claim 10, wherein the second latch comprises a thrid NAND gate and a fourth NAND gate for feeding back each output signal as an input signal each other.

13. The setup/hold time control device according to claim 10, wherein the third latch comprises a fifth NAND gate and a sixth NAND gate for feeding back each output signal as an input signal each other.